ZYNQ7000 FPGA Development Board AC7010/AC7020

User Manual

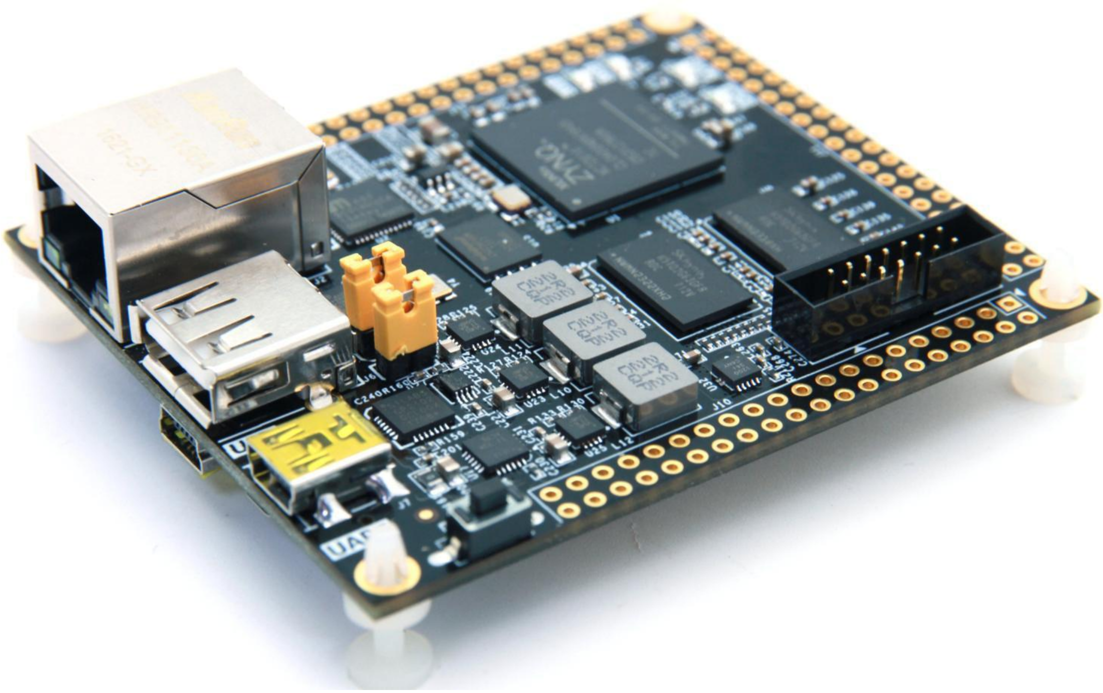
Version Record

Revision	Date	Release By	Description
Rev 1.0	2019-10-01	Rachel Zhou	First Release

Table of Contents

The two core boards of the ALINX XILINX ZYNQ7000 development platform were officially released in 2017, models: AC7010 and AC7020 (industrial grade). Their development platform is the solution for XILINX's Zynq7000 SOC chip. It uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. The AC7010 core board uses Xilinx's Zynq7000 series XC7Z010-1CLG400C as the core processor, and the AC7020 core board uses the industrial grade XC7Z020-2CLG400I chip. Extensive peripheral interfaces such as Gigabit Ethernet, USB2.0, serial port, SD card, etc. are extended on the ARM side. In addition, the core board expands a large number of IOs to the outer three connectors, including 94 IO ports of the PL (47 pairs of LVDS differential) and 8 MIO ports of the PS. For users who need a lot of IO, this core board will be a good choice, and it is also very suitable for secondary development.

The design of the core board adheres to the design concept of “exquisite, practical and concise”. It is not only suitable for the software verification of the software staff, but also suitable for the hardware design of hardware developers, that is, the system cooperation of software and hardware, and accelerated the development process of the project.



Part 1: Introduction

Here, a brief introduction to the ZYNQ7000 core board AC7010/AC7020 is provided.

The core board uses Xilinx's Zynq7000 series of chips, the AC7010 uses the Zynq7000's XC7Z010-1CLG400C chip, and the AC7020 uses the Zynq7000's XC7Z020-2CLG400I chip, both of which are 400-pin FBGA packages. The ZYNQ7000 chip can be divided into a processor system part processor system (PS) and a programmable logic part Programmable Logic (PL).

On the AC7010/AC7020 core board, the PS part of the ZYNQ7000 is equipped with a wealth of external interfaces and devices for user convenience and function verification. The IO ports on the PL side are all led to the 2.54mm connector on the board for user expansion. In addition, there is a 7 x 2 JTAG connector on the core board that can be downloaded and debugged via the ALINX Xilinx USB Cable Downloader. Figure 1-2 shows the structure of the entire AC7010/AC7020 system:

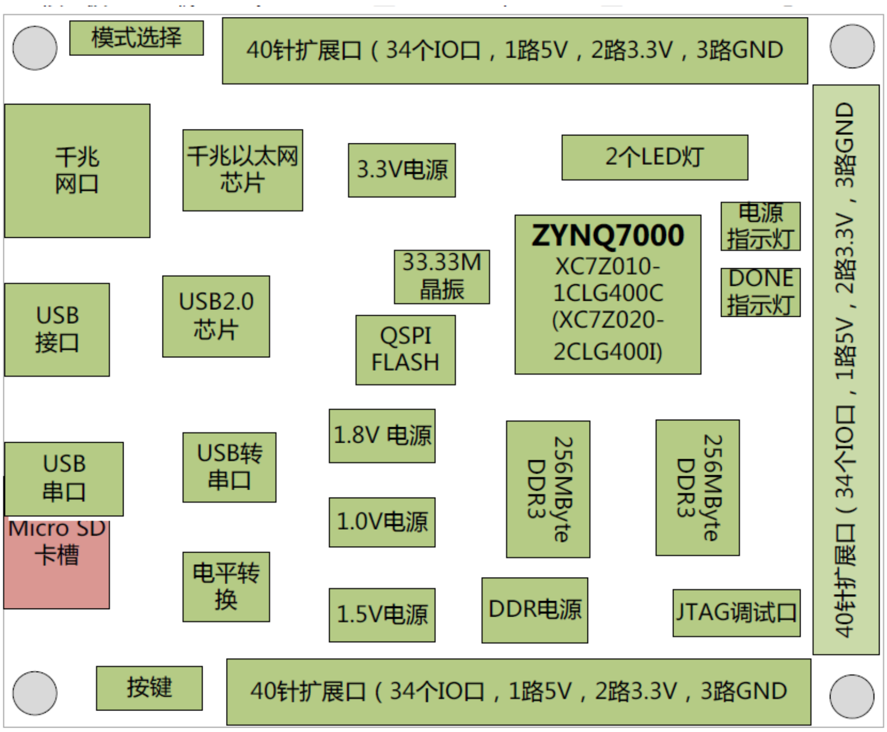


Figure 1-1: The Schematic Diagram of the AC7010/AC7020

Through this diagram, you can see the interfaces and functions that the AC7010/AC7020 FPGA Core Board contains:

- DC5V power input, maximum current does not exceed 500mA
- Xilinx ARM+FPGA chip Zynq-7000 XC7Z010-1CLG400C for AC7010, Zynq-7000 XC7Z020-2CLG400I for AC7020
- DDR3

  Two large-capacity 2Gbit (A total of 4Gbit) high-speed DDR3 SDRAMs can be used as a cache for ZYNQ chip data or as a memory for the operating system
- QSPI FLASH

  A 256Mbit QSPI FLASH memory chip can be used as a Uboot file for ZYNQ chips, storage of system files and user data;
- Gigabit Ethernet Interface

  1-channel 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices.
- USB2.0 HOST Interface

  1-channel USB HOST interface, to connect with external USB slave devices, such as connecting a mouse, keyboard, USB flash drive etc. The USB interface uses a flat USB interface (USB Type A).
- USB OTG Interface

  1-channel high-speed USB2.0 OTG interface for OTG communication with PC or USB devices
- USB Uart Interface

  1-channel USB Uart interface for serial communication with PC or external devices
- LED Light

  2 LEDs, 1 PS control LED, 1 PL control LED.
- Key

  1 reset button for CPU reset

- Clock

  An on-board 33.333Mhz active crystal oscillator provides a stable clock source for the PS system, a 50MHz active crystal oscillator that provides additional clocking for the PL logic

- 3-way 40-pin expansion port (0.1inch Spacing)

  3-way 40-pin 0.1inch spacing expansion port for extending the IOs of ZYNQ PL and PL parts, and can be connect to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.)

- 14-pin JTAG Interface (0.08inch Spacing)

  Used to debug and download the ZYNQ system

- Micro SD card holder

  1-channel Micro SD card holder, to insert SD card for stores operating system images and file systems.

Part 2: Dimensional structure

The size of the development board is 2.95 inch x 2.52 inch, and the PCB is designed with an 8-layer board. There are 4 screw positioning holes around the board for fixing the development board. The holes diameter of the positioning hole is 0.09 inch, and the dxf structure diagram is provided in the documents.

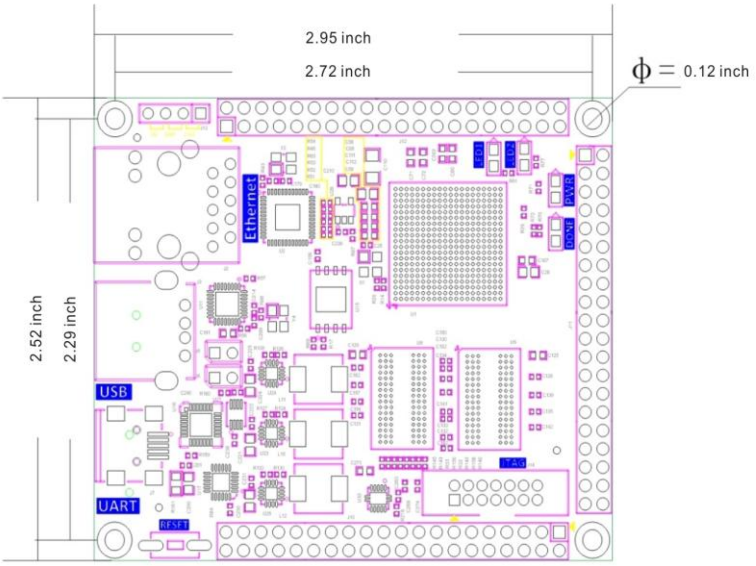


Figure 2-1: FPGA Size Dimension

Part 3: Power Supply

The power input voltage of the development board is DC5V, The schematic diagram of the power supply design on the AX7010 FPGA development board is shown in Figure 3-1

Power input: The core board supply voltage is DC5V. When the core board works alone, connect the USB cable to the USB port of the computer to supply power to the core board. When working with carrier board together, the core board can also be powered through the carrier board. If the AC7010/AC7020 core board is powered by the carrier board, remove the 0Ω resistor (R161) on the board. Please do not use other specifications of the power supply to avoid damage to the core board. The power supply design on the core board is as follows:

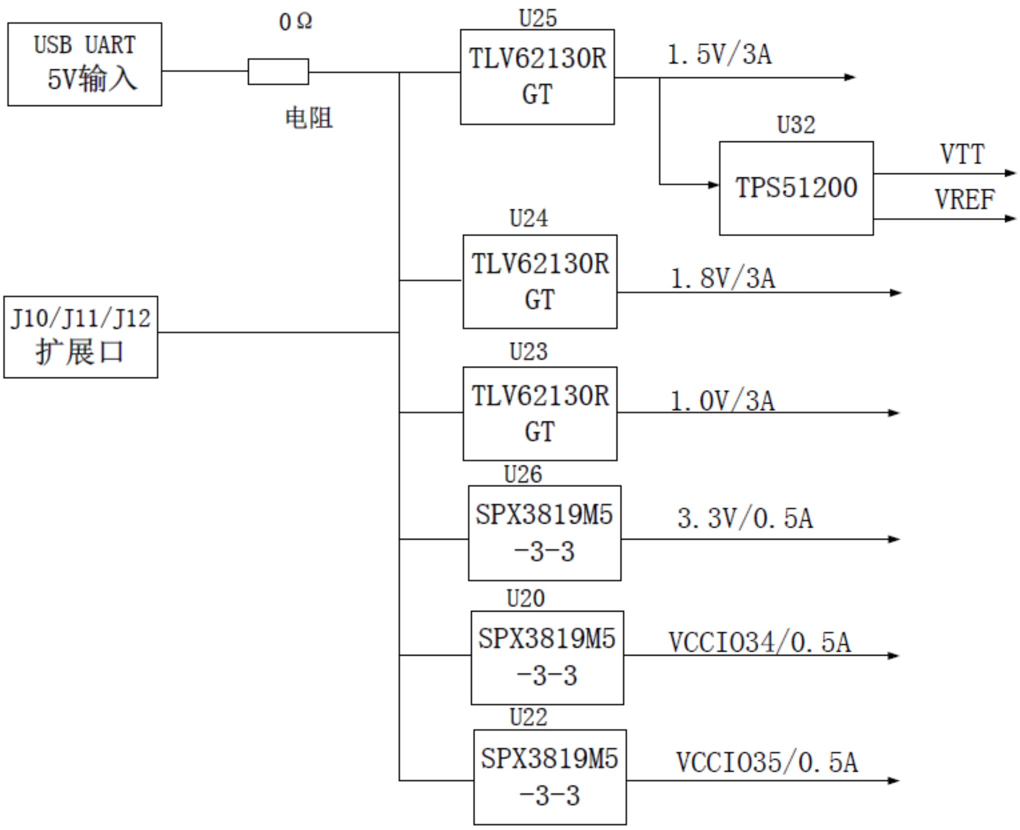


Figure 3-1: Power Supply Schematic

The development board is powered by +5V, and is converted into +1.5V,

+1.8V, +1.0V three-way power supply through three DC/DC power supply chip TLV62130RGT. Each output current can be up to 3A. The 3.3V, VCCIO34 and VCCI35 power supplies are generated by the three LDOs “SPX3819M5-3-3”, the VCCIO34 is powered by the BANK34 of ZYNQ, and the VCCIO35 is powered by the BANK35 of ZYNQ. By replacing with other LDO chips, BANK34 and BANK35IO adapts to different voltage standards. +1.5V Generates VTT and VREF voltages required by DDR3 via TI's TPS51200

The functions of each power distribution are shown in the following table below:

Power Supply	Function
+1.0V	ZYNQ Core Voltage
+1.5V	DDR3, ZYNQ Bank502
+1.8V	ZYNQ auxiliary voltage, ZYNQ PLL, ZYNQ BANK501, VCCIO, Ethernet, USB 2.0
+3.3V	ZYNQ VCCIO, Gigabit Ethernet, Serial Port, HDMI, RTC, FLASH,EEPROM SD Card
VREF, VTT	DDR3
VCCIO34	ZYNQ Bank34
VCCIO35	ZYNQ Bank35

Because the power supply of the PS and PL parts of ZYNQ has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of ZYQN. The power-on sequence is +1.0V->+1.8V->+1.5 V-> (3.3V, VCCIO34, VCCIO35). Figure 3-2 shows the circuit design of the power supply:

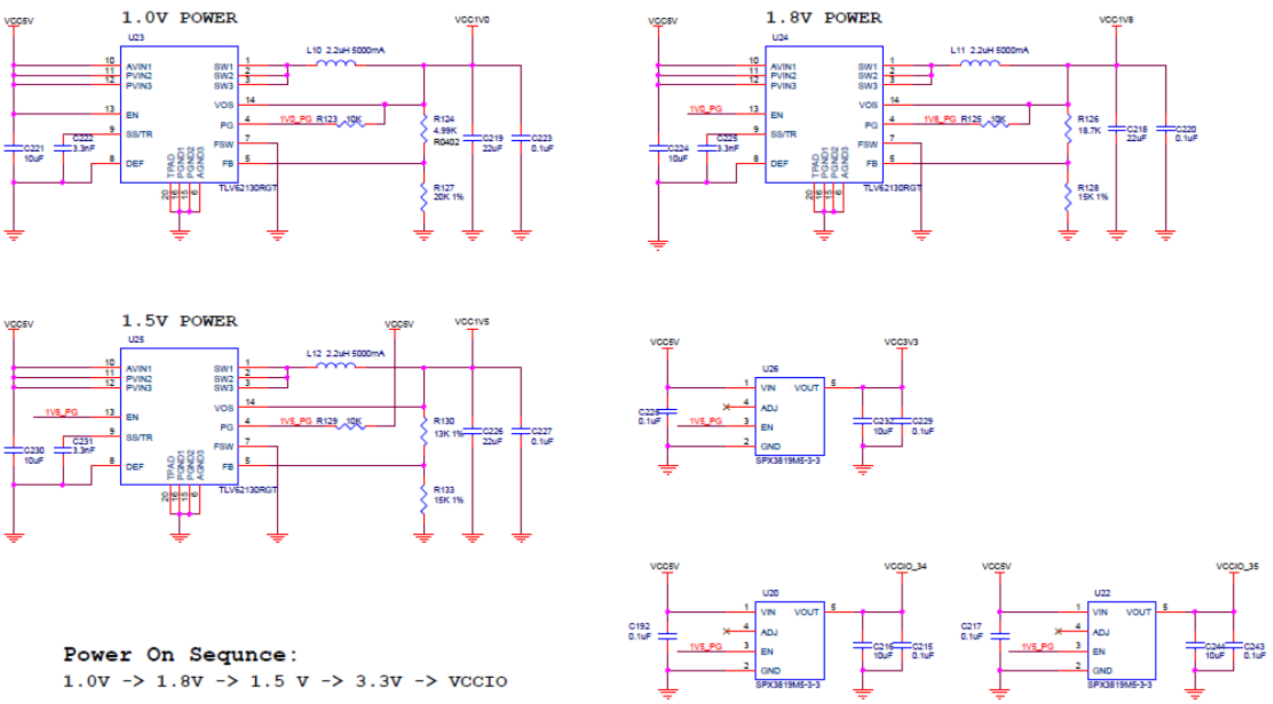


Figure 3-2: Core Board Power Supply Circuit

In the PCB design, an 8-layer PCB is used, and a separate power supply layer and GND layer are reserved, so that the power supply of the entire development board has very good stability.

Part 4: ZYNQ Chip

The Core development board uses Xilinx's Zynq7000 series chip, AC7010 chip model is XC7Z010-1CLG400C (AC7020 chip model is XC7Z020-2CLG400I). The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO etc. The PS can operate independently and start up at power up or reset. Figure 4-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

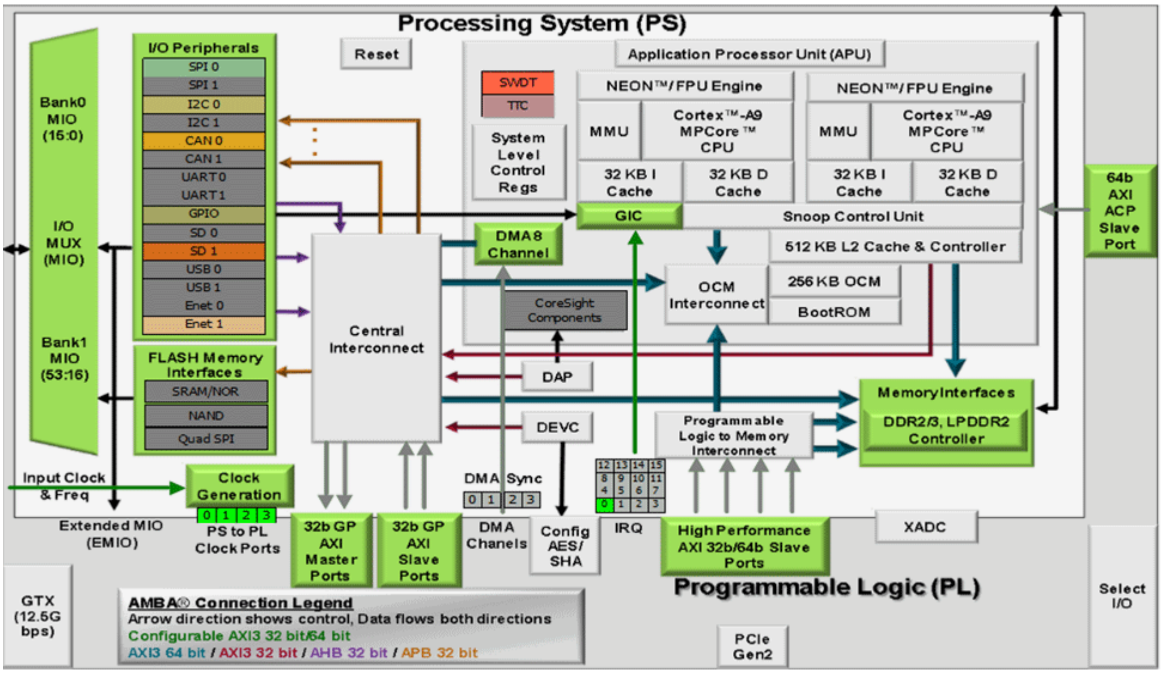


Figure 4-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 800MHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache 2 CPU shares
- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3 interface
- Two Gigabit NIC support: divergent-aggregate DMA, GMII, RGMII, SGMII interface
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 4 sets of 32bit GPIO, 54 (32+22) as PS system IO, 64 connected to PL
- High bandwidth connection within PS and PS to PL

The main parameters of the PL logic part are as follows:

- Logic Cells: 28K
- Look-up-tables (LUTs): 17600
- Flip-flops: 35200
- 18x25MACCs：80
- Block RAM：240KB
- Two AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z010-1CLG400C (or XC7Z020-2CLG400I) chip, package is BGA, 400 pins, the pin pitch is 0.024 inch. Again, let's talk about the BGA pin. When we use the BGA package chip, the pin name becomes in the form of **letters + numbers**, such as E3, G3, etc., Therefore, when we look at the schematic, we see the form of the **letter + number**, which represents the pin of the BGA. Figure 4-2 detailed the XC7Z010 chip on the Core Board AC7010.

Figure 4-2: The XC7Z010 chip on the Core Board AC7010

Part 4.1: JTAG Interface

First, let's talk about the JTAG debug interface (J14) of the AC7010/AC7020 core board. Users can debug and download the ZYNQ program by connecting the ALINX Xilinx USB Cable downloader. Figure 4-3 shows the schematic part of the JTAG port, which involves four signals, TCK, TMS, TDO, and TDI. These four signals are connected to the JTAG pins of BANK0 of the Zynq7010 (Zynq7020) chip (TCK_0, TMS_0, TDO_0 and TDI_0)

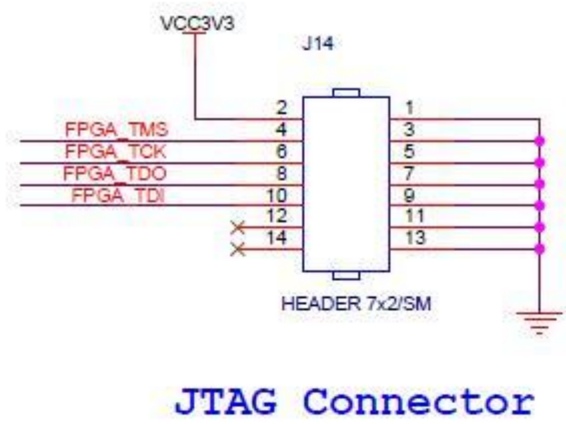


Figure 4-3: The JTAG port schematic

The JTAG interface uses a 14-pin 0.06 inch standard connector, and Figure 4-4 detailed JTAG interface on the core board.

Figure 4-4: The JTAG on the FPGA Core Board

Part 4.2: FPGA Power System

The power supply of the ZYNQ chip is divided into the PS system part and the PL logic part, and the two parts of the power supply work independently.

The power supply of the PS system part and the power supply of the PL logic part have a power-on sequence. The abnormal power-on sequence may cause the ARM system and the FPGA system to not work properly.

The power supply for the PS section is VCCPINT, VCCPAUX, VCCPLL, and PS VCCO. VCCPINT is the PS core power supply pin, connected to 1.0V; VCCPAUX is the PS system auxiliary power supply pin, connected to 1.8V; VCCPLL is the PS internal clock PLL power supply pin, also connected to 1.8V; PS VCCO is BANK voltage, Including VCCO_MIO0, VCCO_MIO1 and VCCO_DDR, depending on the connected peripherals, the connected power supply will be different. On the AC7010/AC7020 FPGA Core Board, VCC_MIO0 is connected to 3.3V, VCCO_MIO1 is connected to 1.8V, and VCCO_DDR is connected to 1.5V. The PS system requires that the power-up sequence be VCCPINT first, then VCCPAUX and VCCPLL, and finally PS VCCO. The order of power outages is reversed.

The power supply for the PL section is VCCINT, VCCBRAM, VCCAUX and VCCO. VCCPINT is the FPGA core power supply pin, connected to 1.0V; VCCBRAM is the power supply pin of the FPGA Block RAM, connected to 1.0V; VCCAUX is the FPGA auxiliary power supply pin, connected to 1.8V; VCCO is the voltage of each BANK of PL, including BANK13, BANK34, BANK35, on the AC7010/AC7020 FPGA Core board, the voltage of BANK is connected to 3.3V. The voltage of BANK34 and BANK35 can be adjusted by replacing the LDO chip. The PL system requires that the power-up sequence be VCCINT first, then VCCBRAM, then VCCAUX, and finally VCCO. If VCCINT and VCCBRAM have the same voltage, they can be powered up at the same time. The order of power outages is reversed.

Part 4.3: ZYNQ boot configuration

The AC7010/AC7020 FPGA Core board supports three boot modes. The three boot modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the ZYNQ7000 chip is powered up, it will detect the level of the responding MIO port to determine which startup mode. Users can select different startup modes through the J13 jumper on the FPGA development board. The J13 startup mode configuration is shown in Table 4-1.

J13	Jump cap position	Start mode
	Connect the left two pins	SD Card
	Connect the middle two pins	QSPI FLASH
	Two pins connected to the right	JTAG

Table 4-1: J13 startup mode configuration

Part 5: Clock Configuration

The AC7010/AC7020 core board provides an active clock for the PS system, and the clock of the PL logic part can be generated by the PLL of the PS part. Alternatively, the 50Mhz crystal oscillator can be used to provide a clock source to achieve separate operation of the PS system and PL logic.

Part 5.1: PS system clock source

The ZYNQ chip provides a 33.333MHz clock input to the PS section via the X1 crystal on the FPGA core board. The input of the clock is connected to the pin of the PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 5-1:

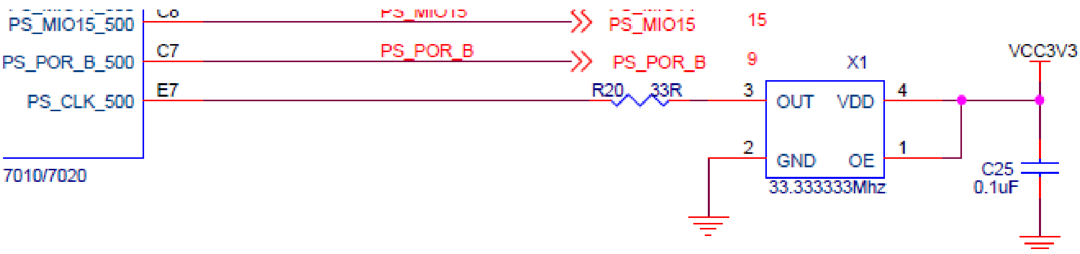


Figure 5-1: Active crystal oscillator to the PS section

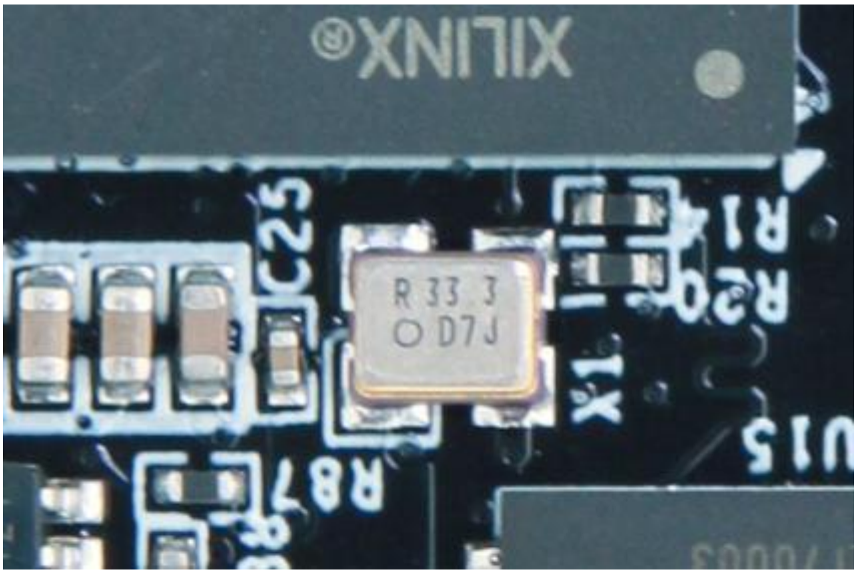


Figure 5-2: 33.333Mhz active Crystal Oscillator on the FPGA board

PS Clock Pin Assignment

Signal Name	ZYNQ Pin
PS_CLK_500	E7

Part 5.2: PL system clock source

The AC7010/AC7020 FPGA core board, The PL system clock on the AC7010/AC7020 core board is powered by a 50MHz active crystal. This 50Mhz clock can be used to drive user logic in the FPGA. The schematic diagram of the clock source is shown in Figure 5-3.

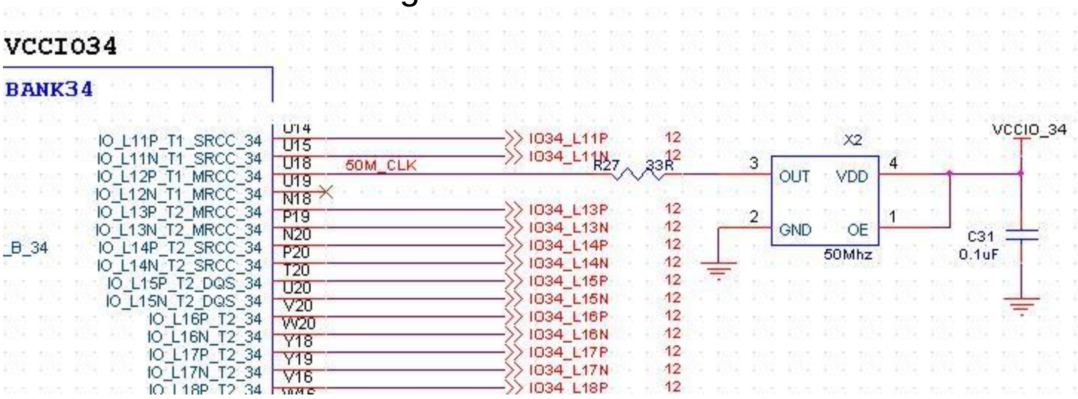


Figure 5-3: PL system clock source

PL Clock pin assignment:

Signal Name	ZYNQ Pin
500_CLK	U18

Part 6：ZYNQ Processor System (PS) peripherals

ZYNQ is composed of the PS part of the ARM system and the PL part of the FPGA logic. Some peripherals on the FPGA core board are connected to the IO of the PS, and some peripherals are connected to the IO of the PL. First introduce the peripherals connected to the PS part.

Part 6.1: QSPI Flash

The AC7010/AC7020 FPGA core board is equipped with a 256MBit Quad-SPI FLASH chip, model W25Q256, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 6-1.

Position	Model	Capacity	Factory
U6	W25Q256BV	32M Byte	Winbond

Table 6-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 6-1 shows the QSPI Flash in the schematic.

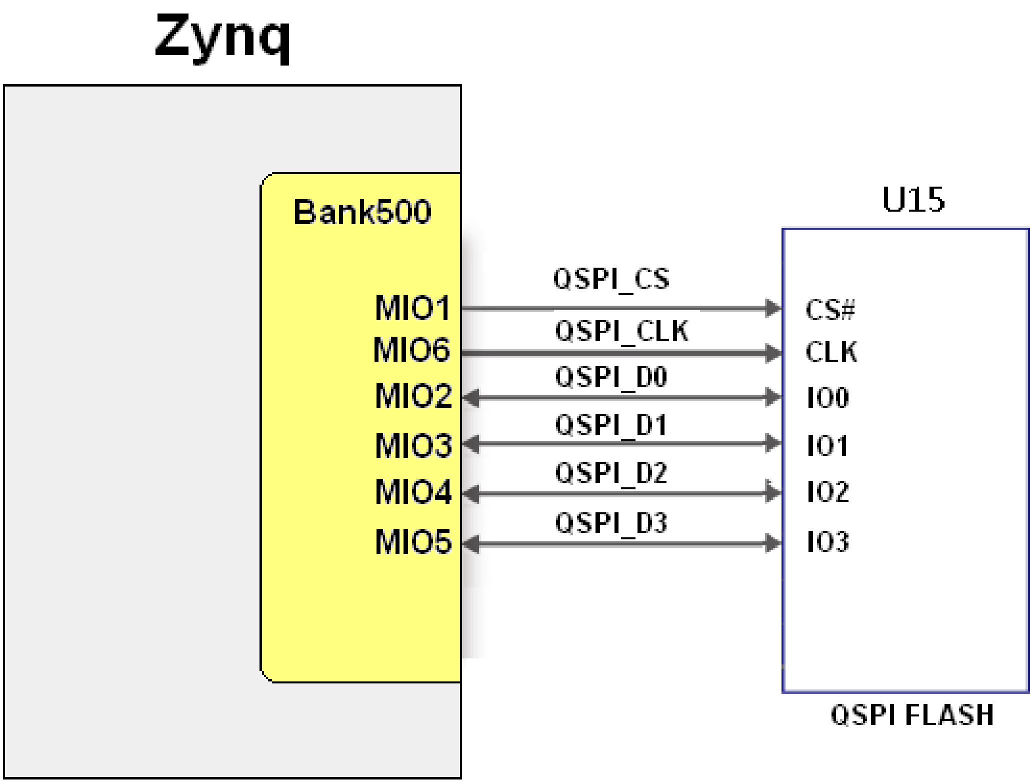


Figure 6-1: QSPI Flash Connection Diagram

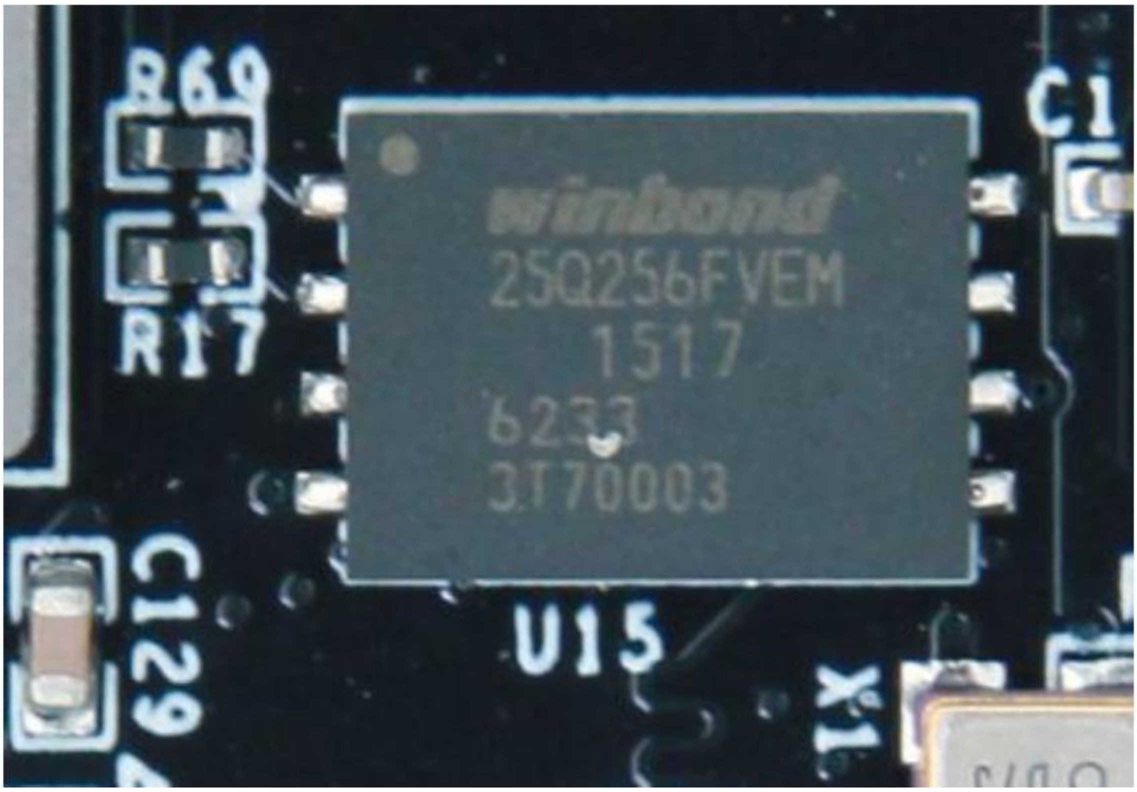


Figure 6-2: QSPI Flash on AC7010/AC7020 FPGA Core Board

Configure chip pin assignments:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
QSPI_SCK	PS_MIO6_500	A5
QSPI_CS	PS_MIO1_500	A7
QSPI_D0	PS_MIO2_500	B8
QSPI_D1	PS_MIO3_500	D6
QSPI_D2	PS_MIO4_500	B7
QSPI_D3	PS_MIO5_500	A6

Part 6.2: DDR3 DRAM

The AC7010 FPGA core board is equipped with two SKHynix 2Gbit DDR3 chips (total 4Gbit), model H5TQ2G63FFR-RDC (compatible with MT41J128M16HA-125). The AC7020 FPGA core board is equipped with two SKHynix 4Gbit DDR3 chips (total 8Gbit), model H5TQ4G63AFR-PBI (compatible with MT41J256M16RE-125).

The bus width of DDR is 32bits in total, and the maximum operating speed of DDR3 SDRAM is 533MHz (data rate 1066Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 502 of the ZYNQ Processing System (PS). The specific configuration of DDR3 SDRAM is shown in Table 6-2.

Core Board	Bit Number	Chip Model	Capacity	Factory
AC7010	U8,U9	H5TQ2G63FFR-RDC	128M x 16bit	SKhynix
AC7020	U8,U9	H5TQ4G63AFR-PBI	256M x 16bit	SKhynix

Table 6-2: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

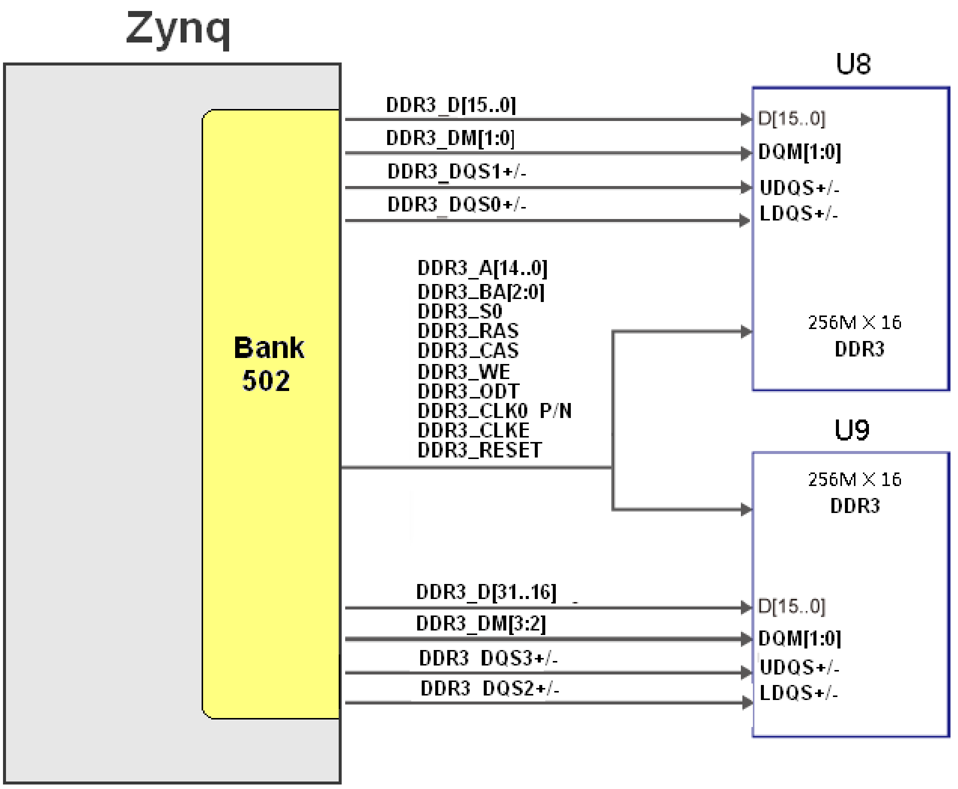


Figure 6-2: The Schematic Part of DDR3 DRAM

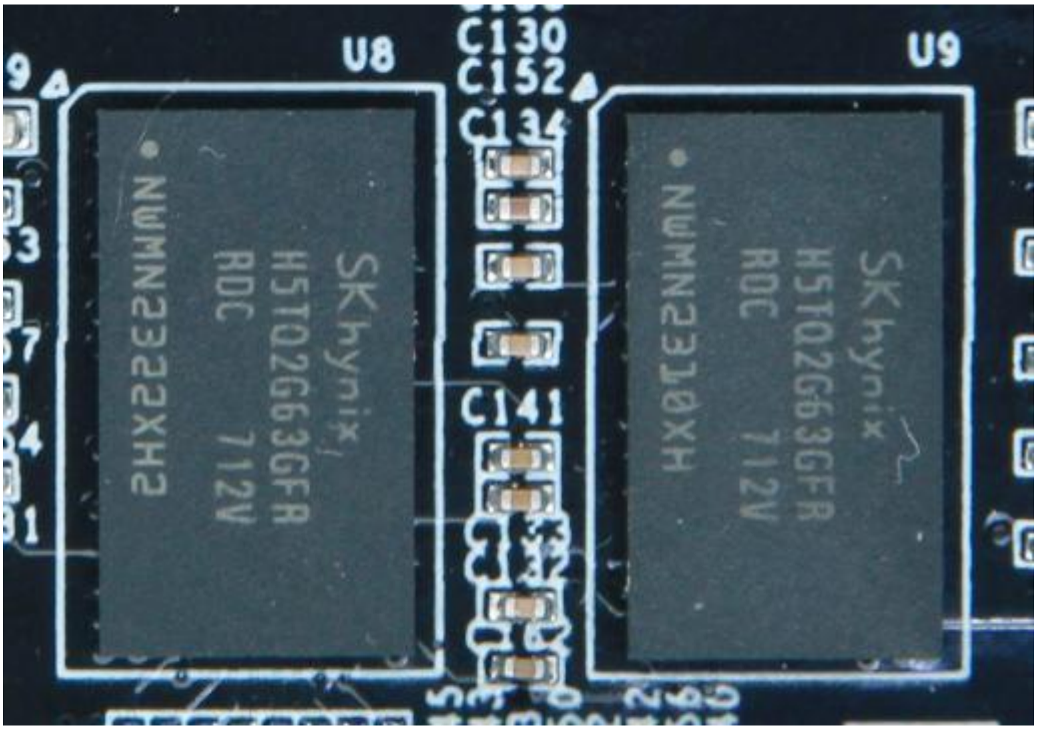


Figure 6-3: Two DDR3 DRAMs on the FPGA Core Board

DDR3 Pin Assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3_DQS0_N	PS_DDR_DQS_N0_502	B2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	G2
DDR3_DQS1_N	PS_DDR_DQS_N1_502	F2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	R2
DDR3_DQS2_N	PS_DDR_DQS_N2_502	T2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	W5
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W4
DDR3_DQ[0]	PS_DDR_DQ0_502	C3
DDR3_DQ [1]	PS_DDR_DQ1_502	B3
DDR3_DQ [2]	PS_DDR_DQ2_502	A2
DDR3_DQ [3]	PS_DDR_DQ3_502	A4
DDR3_DQ [4]	PS_DDR_DQ4_502	D3
DDR3_DQ [5]	PS_DDR_DQ5_502	D1
DDR3_DQ [6]	PS_DDR_DQ6_502	C1
DDR3_DQ [7]	PS_DDR_DQ7_502	E1
DDR3_DQ [8]	PS_DDR_DQ8_502	E2
DDR3_DQ [9]	PS_DDR_DQ9_502	E3
DDR3_DQ [10]	PS_DDR_DQ10_502	G3
DDR3_DQ [11]	PS_DDR_DQ11_502	H3
DDR3_DQ [12]	PS_DDR_DQ12_502	J3
DDR3_DQ [13]	PS_DDR_DQ13_502	H2
DDR3_DQ [14]	PS_DDR_DQ14_502	H1
DDR3_DQ [15]	PS_DDR_DQ15_502	J1
DDR3_DQ [16]	PS_DDR_DQ16_502	P1
DDR3_DQ [17]	PS_DDR_DQ17_502	P3
DDR3_DQ [18]	PS_DDR_DQ18_502	R3
DDR3_DQ [19]	PS_DDR_DQ19_502	R1
DDR3_DQ [20]	PS_DDR_DQ20_502	T4
DDR3_DQ [21]	PS_DDR_DQ21_502	U4
DDR3_DQ [22]	PS_DDR_DQ22_502	U2
DDR3_DQ [23]	PS_DDR_DQ23_502	U3
DDR3_DQ [24]	PS_DDR_DQ24_502	V1
DDR3_DQ [25]	PS_DDR_DQ25_502	Y3

DDR3_DQ [26]	PS_DDR_DQ26_502	W1
DDR3_DQ [27]	PS_DDR_DQ27_502	Y4
DDR3_DQ [28]	PS_DDR_DQ28_502	Y2
DDR3_DQ [29]	PS_DDR_DQ29_502	W3
DDR3_DQ [30]	PS_DDR_DQ30_502	V2
DDR3_DQ [31]	PS_DDR_DQ31_502	V3
DDR3_DM0	PS_DDR_DM0_502	A1
DDR3_DM1	PS_DDR_DM1_502	F1
DDR3_DM2	PS_DDR_DM2_502	T1
DDR3_DM3	PS_DDR_DM3_502	Y1
DDR3_A[0]	PS_DDR_A0_502	N2
DDR3_A[1]	PS_DDR_A1_502	K2
DDR3_A[2]	PS_DDR_A2_502	M3
DDR3_A[3]	PS_DDR_A3_502	K3
DDR3_A[4]	PS_DDR_A4_502	M4
DDR3_A[5]	PS_DDR_A5_502	L1
DDR3_A[6]	PS_DDR_A6_502	L4
DDR3_A[7]	PS_DDR_A7_502	K4
DDR3_A[8]	PS_DDR_A8_502	K1
DDR3_A[9]	PS_DDR_A9_502	J4
DDR3_A[10]	PS_DDR_A10_502	F5
DDR3_A[11]	PS_DDR_A11_502	G4
DDR3_A[12]	PS_DDR_A12_502	E4
DDR3_A[13]	PS_DDR_A13_502	D4
DDR3_A[14]	PS_DDR_A14_502	F4
DDR3_BA[0]	PS_DDR_BA0_502	L5
DDR3_BA[1]	PS_DDR_BA1_502	R4
DDR3_BA[2]	PS_DDR_BA2_502	J5
DDR3_S0	PS_DDR_CS_B_502	N1
DDR3_RAS	PS_DDR_RAS_B_502	P4
DDR3_CAS	PS_DDR_CAS_B_502	P5
DDR3_WE	PS_DDR_WE_B_502	M5
DDR3_ODT	PS_DDR_ODT_502	N5
DDR3_RESET	PS_DDR_DRST_B_502	B4
DDR3_CLK_P	PS_DDR_CKP_502	L2
DDR3_CLK_N	PS_DDR_CKN_502	M2

DDR3_CKE	PS_DDR_CKE_502	N3

Part 6.3: Gigabit Ethernet Interface

The AC7010/AC7020 FPGA core board provides network communication services to users through Micrel's KSZ9031RNX Ethernet PHY chip. The Ethernet PHY chip is connected to the GPIO interface of the PSNK 501 of the ZYNQ. The KSZ9031RNX chip supports 10/100/1000 Mbps network transmission rate and communicates with the MAC layer of the Zynq7000 PS system through the RGMII interface. KSZ9031RNX supports MDI/MDX adaptation, various speed self-adjustment, Master/Slave adaptation, and supports MDIO bus for PHY register management. The KSZ9031RNX power-on will detect the level status of some specific IOs to determine their working mode.

Table 6-2 describes the default setup information after the GPHY chip is powered up.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address is 001
CLK125_EN	Enable 125Mhz clock output selection	Enable
LED_MODE	LED mode configuration	Single LED mode
MODE0~MODE3	Link adaptation and full duplex configuration	10/100/1000 adaptive, compatible with full-duplex, half-duplex

Table 6-2: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip KSZ9031RNX is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip KSZ9031RNX is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

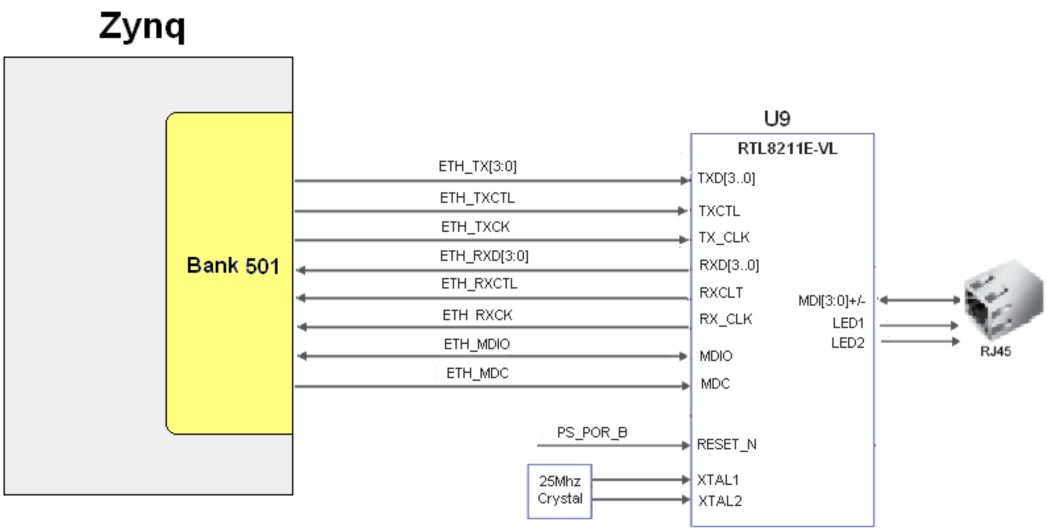


Figure 6-4: The connection of the ZYNQ and GPHY chip

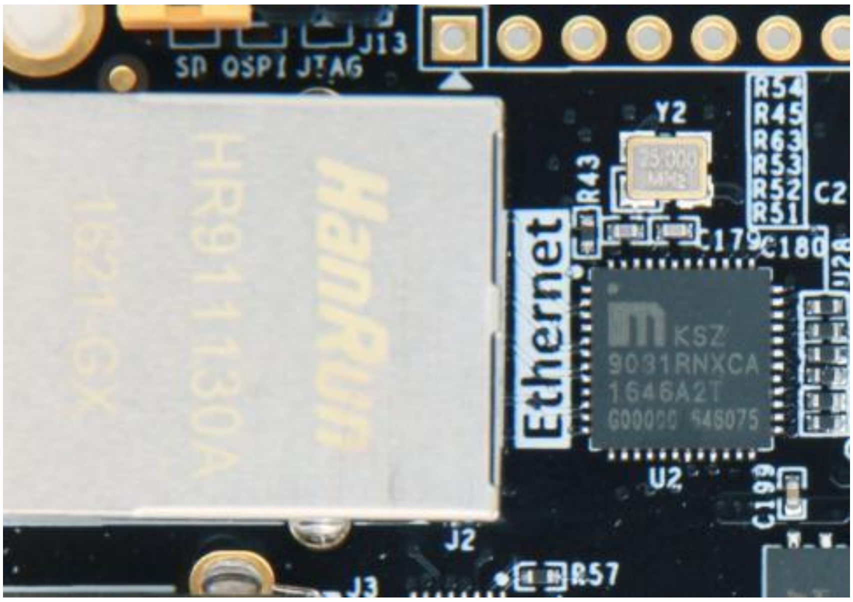


Figure 6-5: The GPHY chip on FPGA Board

The Gigabit Ethernet pin assignments are as follows:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
ETH_GCLK	PS_MIO16_501	A19	RGMII Transmit Clock
ETH_TXD0	PS_MIO17_501	E14	Transmit data bit0
ETH_TXD1	PS_MIO18_501	B18	Transmit data bit1
ETH_TXD2	PS_MIO19_501	D10	Transmit data bit2
ETH_TXD3	PS_MIO20_501	A17	Transmit data bit3
ETH_TXCTL	PS_MIO21_501	F14	Transmit enable signal

ETH_RXCK	PS_MIO22_501	B17	RGMII Receive Clock
ETH_RXD0	PS_MIO23_501	D11	Receive data Bit0
ETH_RXD1	PS_MIO24_501	A16	Receive data Bit1
ETH_RXD2	PS_MIO25_501	F15	Receive data Bit2
ETH_RXD3	PS_MIO26_501	A15	Receive data Bit3
ETH_RXCTL	PS_MIO27_501	D13	Receive data valid signal
ETH_MDC	PS_MIO52_501	C10	MDIO Management clock
ETH_MDIO	PS_MIO53_501	C11	MDIO Management data

Part 6.4: USB2.0 Interface

The USB2.0 transceiver used in the AC7010/AC7020 is a 1.8V, high-speed USB3320C-EZK that supports the ULPI standard interface. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver for high-speed USB2.0 Host mode and Slave mode data communication. The USB3320C's USB data and control signals are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip. A 24MHz crystal provides the system clock for the USB3320C.

The core board provides users with two USB ports, one is the Host USB port and the other is the OTG USB port. They are a flat USB interface (USB Type A) and a micro USB interface (Micro USB), which are convenient for users to connect different USB peripherals. Users can switch between Host and OTG through J5 and J6 jumpers on the core board. Table 6-3 shows the mode switching instructions:

J5,J6 Status	USB Mode	Instruction
J5 and J6 installation jumper caps	HOST Mode	FPGA core board as the main device, USB port to connect the mouse, keyboard, USB and other slave peripherals
J5 and J6 not installation jumper caps	OTG Mode	FPGA core board as a slave device, USB port to connect to the computer

Table 6-3: The USB interface mode switching instructions

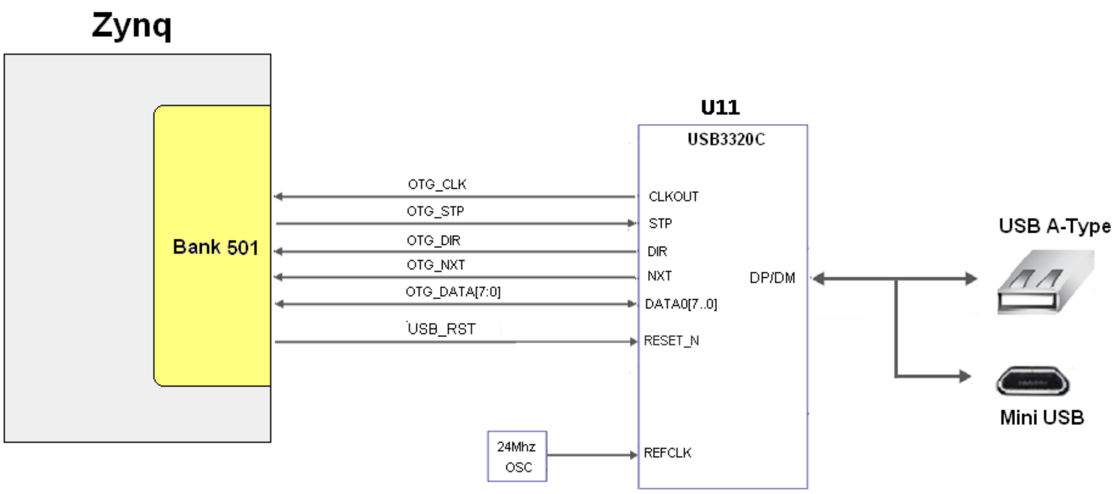


Figure 6-6: The connection between Zynq7000 and USB chip

Figure 6-7 shows the physical diagram of the USB2.0 part. U11 is USB3320C, J3 is the Host USB interface, and J4 is the OTG USB interface. Jumper caps J5 and J6 are used for Host and OTG mode selection.

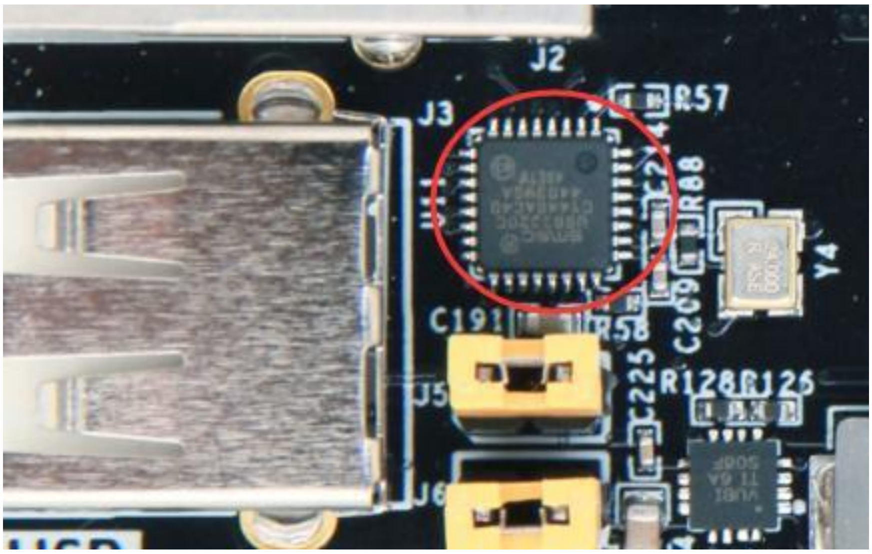


Figure 6-7: The USB3320C chip on the FPGA Board

USB2.0 Pin Assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
OTG_DATA4	PS_MIO28_501	C16	USB Data Bit4
OTG_DIR	PS_MIO29_501	C13	USB Data Direction Signal
OTG_STP	PS_MIO30_501	C15	USB Stop Signal

OTG_NXT	PS_MIO31_501	E16	USB Next Data Signal
OTG_DATA0	PS_MIO32_501	A14	USB Data Bit0
OTG_DATA1	PS_MIO33_501	D15	USB Data Bit1
OTG_DATA2	PS_MIO34_501	A12	USB Data Bit2
OTG_DATA3	PS_MIO35_501	F12	USB Data Bit3
OTG_CLK	PS_MIO36_501	A11	USB Clock Signal
OTG_DATA5	PS_MIO37_501	A10	USB Data Bit5
OTG_DATA6	PS_MIO38_501	E13	USB Data Bit6
OTG_DATA7	PS_MIO39_501	C18	USB Data Bit7
OTG_RESETN	PS_MIO46_501	D16	USB Reset Signal

Part 6.5: USB to Serial Port

The AC7100/AC7200 FPGA development board uses the USB to UART chip of Silicon Labs CP2102GM. The USB interface uses the Micro USB interface. Users can connect to the PC for serial communication using a Micro USB cable.

The TX/RX signal of the UART is connected to the signal of the PS BANK501 of the ZYNQ EPP. Since the VCCMIO of the BANK is set to 1.8V, the data level of the CP2102GM is 3.3V, which is connected by the TXS0102DCUR level conversion chip. Figure 6-8 detailed the schematic diagram of the CP2102GM and ZYNQ connections

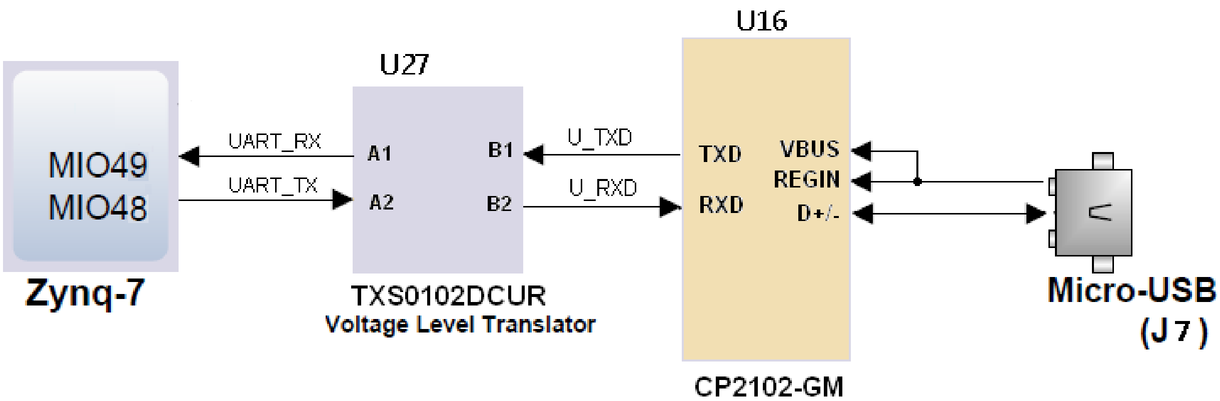


Figure 6-8: CP2102GM Connection Diagram

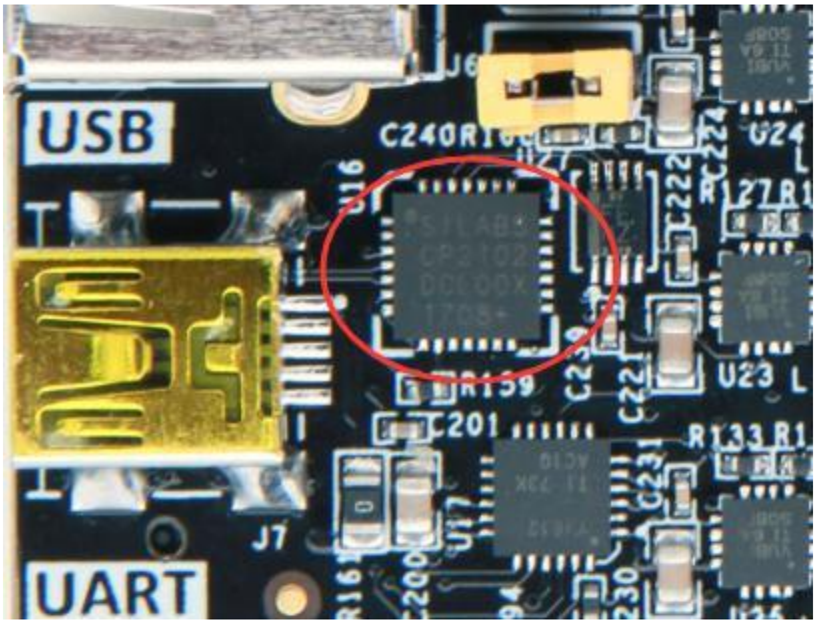


Figure 6-9: CP2102GM chip on the FPGA Core Board

USB to serial port ZYNQ pin assignment:

Signal name	ZYNQ Pin Name	ZYNQ Pin Number	Description
UART_TX	PS_MIO48_501	B12	Uart data input
UART_RX	PS_MIO49_501	C12	Uart data output

Silicon Labs provides virtual COM port (VCP) drivers for host PCs. These drivers allow the CP2102GM USB-UART bridge device to be displayed as a COM port in communications application software, such as TeraTerm or HyperTerminal. The VCP device driver must be installed before the PC host establishes communication with the AC7010/AC7020 FPGA core board.

Part 6.6: SD Card Slot

The AC7010/AC7020 core board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for storing the ZYNQ chip, the Linux operating system kernel, the file system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the

SD card is 3.3V, connected through the TXS02612 level shifter. The schematic of the Zynq7000 PS and SD card connector is shown in Figure 6-10:

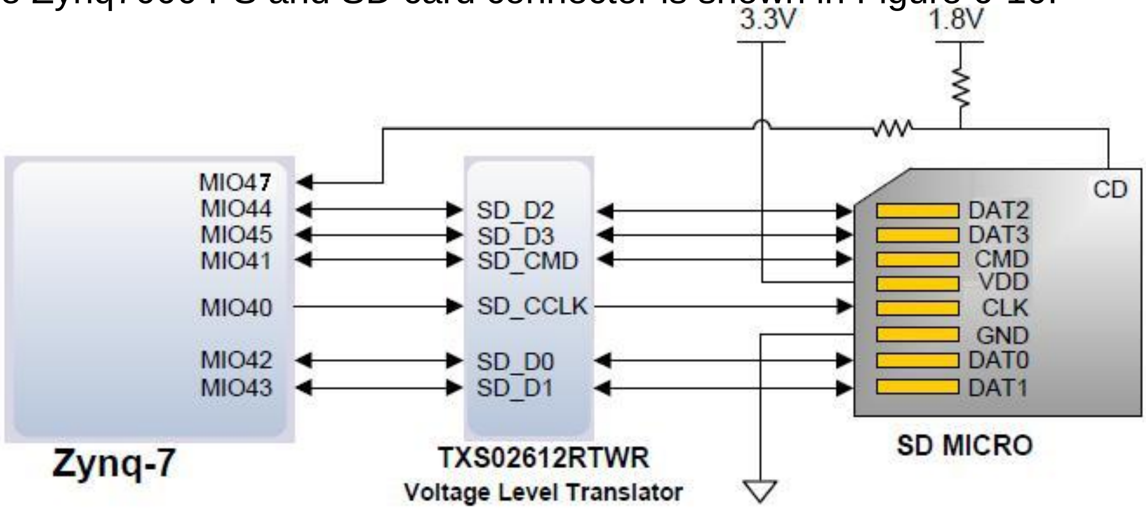


Figure 6-10: SD Card Connection Diagram

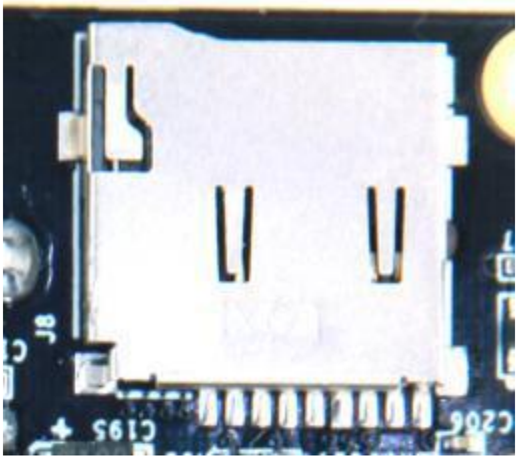


Figure 6-11: SD Card Slot on the FPGA Board

SD card slot pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SD_CLK	PS_MIO40	D14	SD Clock Signal
SD_CMD	PS_MIO41	C17	SD Command Signal
SD_D0	PS_MIO42	E12	SD Data0
SD_D1	PS_MIO43	A9	SD Data1
SD_D2	PS_MIO44	F13	SD Data2
SD_D3	PS_MIO45	B15	SD Data3
SD_CD	PS_MIO47	B14	SD Card Insertion Signal

Part 6.7: User LEDs

On the AC7010/AC7020 core board, one LED light-emitting diode is connected to the BANK500 IO of the PS part, and the user can use this LED light to debug the program. When the BANK500 IO voltage is high, the LED light is off, and when the BANK500 IO voltage is low, the LED will be illuminated. Figure 6-14 shows the connection between ZYNQ BANK500 IO and LED lights.

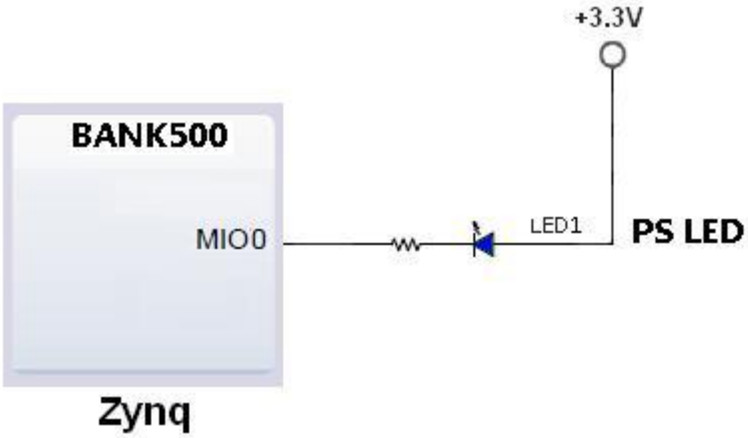


Figure 6-12: Zynq-7000 and LED connection diagram

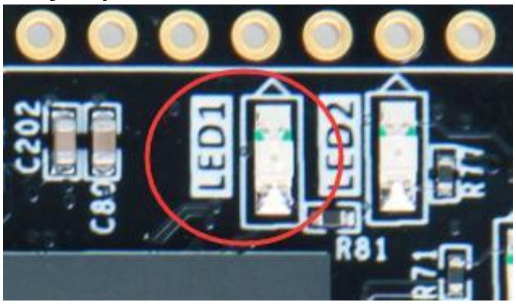


Figure 6-13: PS User LEDs on the FPGA Core Board

PS User LEDs pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
MIO0_LED	PS_MIO0_500	E6	PS User LED LED1

Part 6.8: Reset Key

On the AC7010/AC7020 core board, the entire ZYNQ system is reset by a RESET key, and the reset signal is connected to the PS pin's reset pin PS_POR_B_500. The user can use this user key to manually reset. In the design, when the reset key is pressed, the reset signal is low, and the ZYNQ chip is reset. When the key is released, the ZYNQ chip starts to work normally. Figure 6-16 shows the reset key connection:

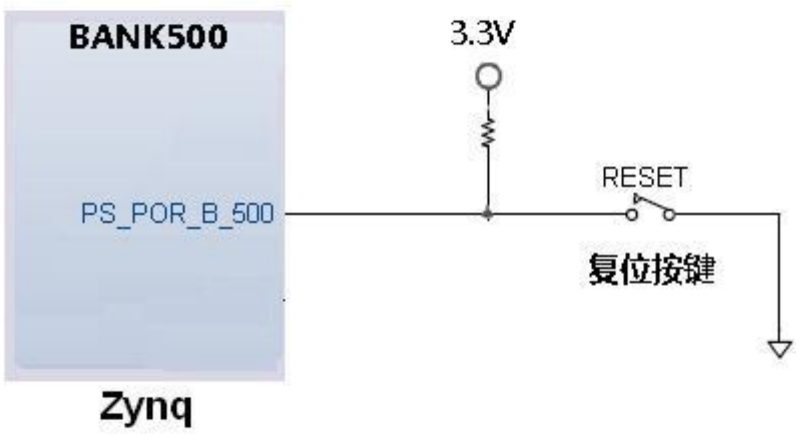


Figure 6-14: Zynq-7000 and PS Key connection diagram

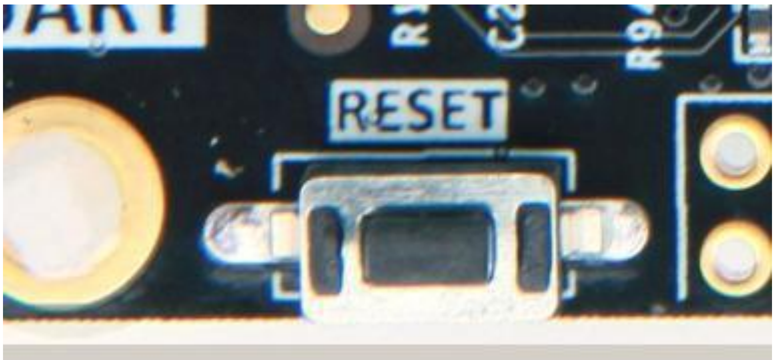


Figure 6-15: PS Reset Key on the FPGA Board

PS Reset Key pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
PS_POR_B	PS_POR_B _500	C7	PS Reset Key

Part 7：ZYNQ PL Peripherals

Part 7.1: User LEDs

The PL part of the AC7010/AC7020 FPGA core board is also connected to one LED light-emitting diode. The schematic diagram is shown in Figure 7-1, The LED signal is connected to the IO of the PL part BANK34. When the IO output of the PL part BANK34 is logic 0, the LED will be illuminated. When it is logic 1, the LED will be extinguished.

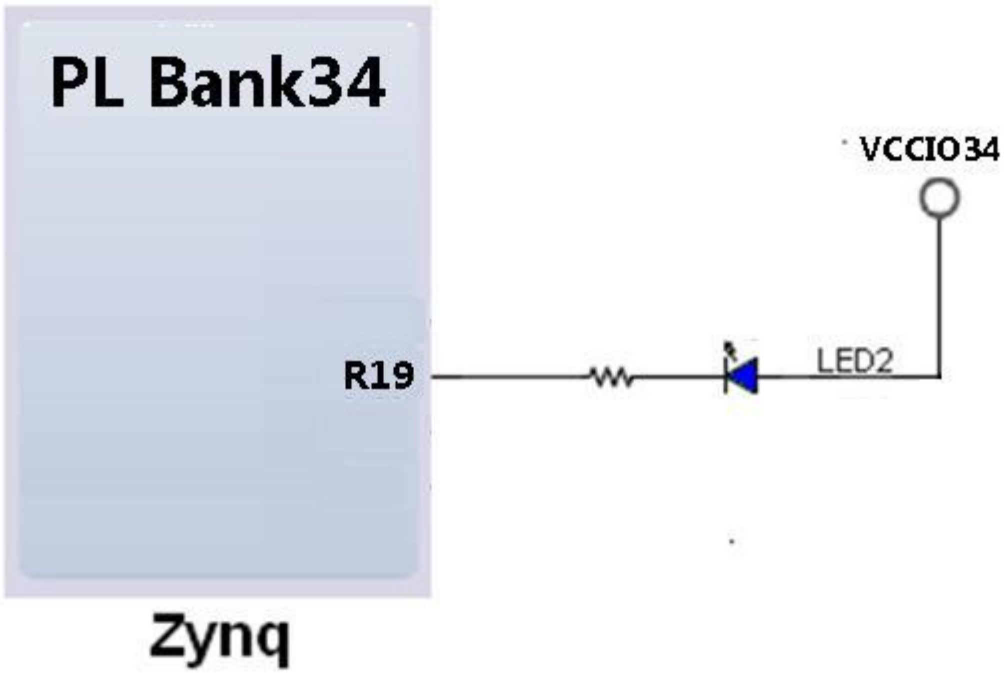


Figure 7-1: PL User LED Schematic

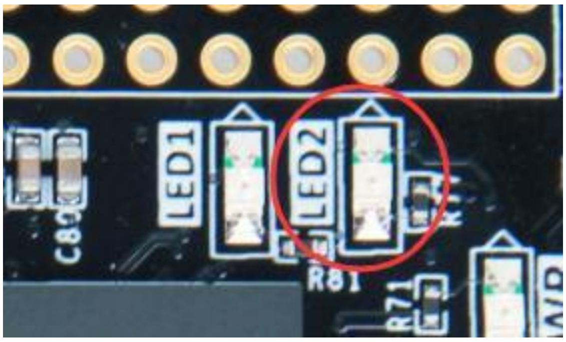


Figure 7-2: PL User LEDs on the FPGA Core Board

PL User LEDs pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
LED2	IO_0_34	R19	PL User LED PL LED2

Part 7.2: Expansion Port J10

The expansion port J10 is a 40-pin 2.54mm double-row connector, which expands more peripherals and interfaces for users. The default is not soldered, the user can solder to a double-row male connectors or female connectors as needed.

The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. Among the 34 IO signals, 26 of them are connected to the IO of the BANK34 of the ZYNQ PL. The PCB design is differentially connected. The default level is 3.3V. The user can change the IO level of the BANK34 by replacing the power chip (U20) on the core board. In addition, there are 8 IO ports connected to the MIO of the PS terminal, and the level standard is 3.3V.

Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.

The circuit of the expansion port (J10) is shown in Figure 7-3:

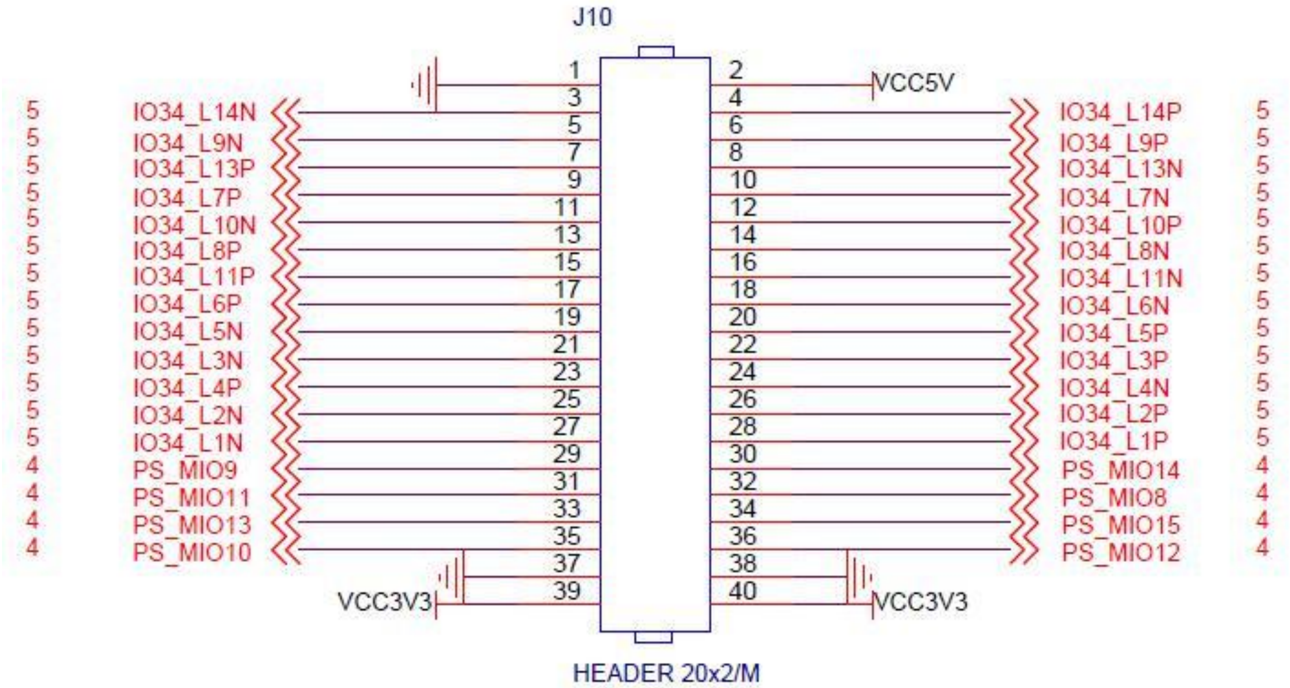


Figure 7-3: Expansion header J10 schematic

Figure 7-4: Expansion header J10 on the FPGA Board

J10 Expansion Header Pin Assignment

J10 Pin	Signal Name	ZYNQ Pin Number
PIN1	GND	-
PIN2	+5V	-
PIN3	IO34_L14N	P20
PIN4	IO34_L14P	N20
PIN5	IO34_L9N	U17
PIN6	IO34_L9P	T16
PIN7	IO34_L13P	N18
PIN8	IO34_L13N	P19
PIN9	IO34_L7P	Y16
PIN10	IO34_L7N	Y17
PIN11	IO34_L10N	W15
PIN12	IO34_L10P	V15
PIN13	IO34_L8P	W14
PIN14	IO34_L8N	Y14
PIN15	IO34_L11P	U14
PIN16	IO34_L11N	U15
PIN17	IO34_L6P	P14
PIN18	IO34_L6N	R14
PIN19	IO34_L5N	T15
PIN20	IO34_L5P	T14
PIN21	IO34_L3N	V13
PIN22	IO34_L3P	U13
PIN23	IO34_L4P	V12
PIN24	IO34_L4N	W13
PIN25	IO34_L2N	U12
PIN26	IO34_L2P	T12
PIN27	IO34_L1N	T10
PIN28	IO34_L1P	T11
PIN29	PS_MIO9	B5
PIN30	PS_MIO14	C5
PIN31	PS_MIO11	C6
PIN32	PS_MIO8	D5
PIN33	PS_MIO13	E8
PIN34	PS_MIO15	C8

PIN35	PS_MIO10	E9
PIN36	PS_MIO12	D9
PIN37	GND	-
PIN38	GND	-
PIN39	+3.3V	-
PIN40	+3.3V	-

Part 7.3: Expansion Port J11

The expansion port J11 is a 40-pin 0.1 inch double-row connector, which expands more peripherals and interfaces for users. The default is not soldered, the user can solder to a double-row male connectors or female connectors as needed. The J11 interface can be directly connected to the module provided by ALINX. The expansion port J11, which expands more peripherals and interfaces for users. Currently, the J11 interface can be directly connected to the module provided by ALINX, include: ADDA module, LCD module, Gigabit Ethernet module, audio input/output module, matrix keyboard module, 500W binocular vision camera module, etc.

The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. 34 IO ports are connected to BANK34 and BANK35 of ZYNQ PL. The PCB design is differentially connected. The default level is 3.3V. The user can change the level of IO by replacing the power chip (SPX3819M5-3-3) of VCCIO34 and VCCIO35 on the core board.

Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.

The circuit of the expansion port (J11) is shown in Figure 7-5:

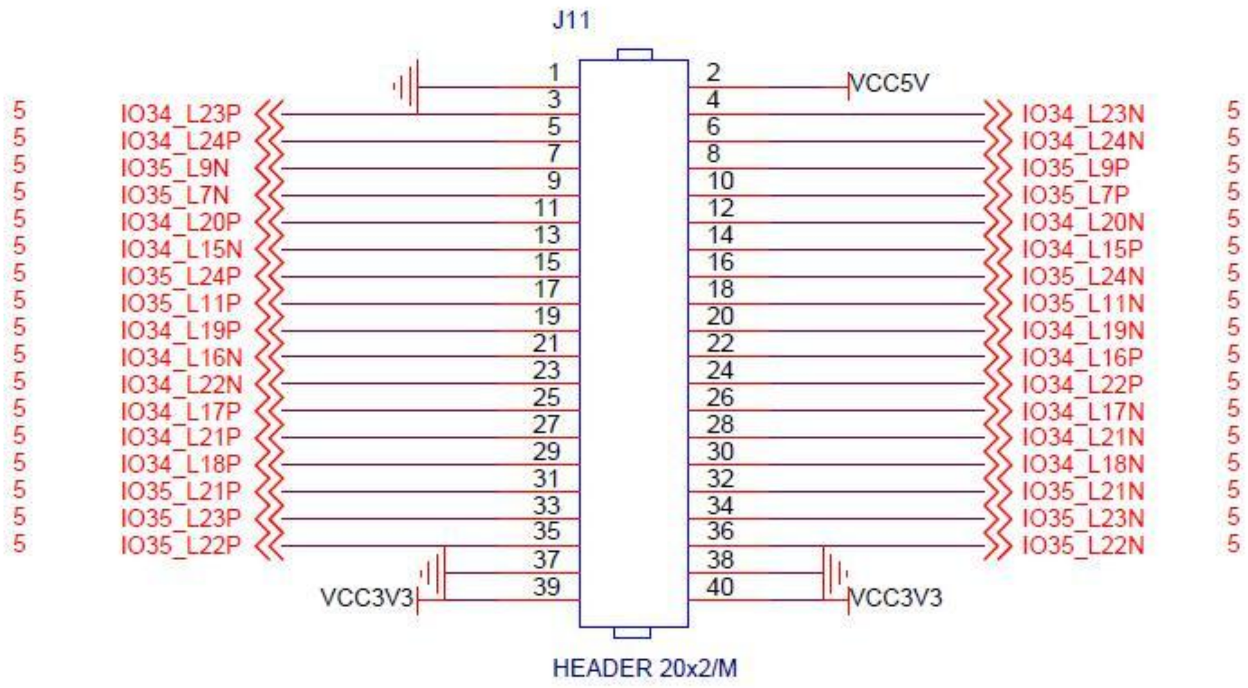


Figure 7-5: Expansion Port J11 schematic

Figure 7-6: Expansion header J11 on the FPGA Board

J11 Expansion Header Pin Assignment

J11 Pin	Signal Name	ZYNQ Pin Number
PIN1	GND	-
PIN2	+5V	-
PIN3	IO34_L23P	N17
PIN4	IO34_L23N	P18
PIN5	IO34_L24P	P15
PIN6	IO34_L24N	P16
PIN7	IO35_L9N	L20
PIN8	IO35_L9P	L19
PIN9	IO35_L7N	M20
PIN10	IO35_L7P	M19
PIN11	IO34_L20P	T17
PIN12	IO34_L20N	R18
PIN13	IO34_L15N	U20

PIN14	IO34_L15P	T20
PIN15	IO35_L24P	K16
PIN16	IO35_L24N	J16
PIN17	IO35_L11P	L16
PIN18	IO35_L11N	L17
PIN19	IO34_L19P	R16
PIN20	IO34_L19N	R17
PIN21	IO34_L16N	W20
PIN22	IO34_L16P	V20
PIN23	IO34_L22N	W19
PIN24	IO34_L22P	W18
PIN25	IO34_L17P	Y18
PIN26	IO34_L17N	Y19
PIN27	IO34_L21P	V17
PIN28	IO34_L21N	V18
PIN29	IO34_L18P	V16
PIN30	IO34_L18N	W16
PIN31	IO35_L21P	N15
PIN32	IO35_L21N	N16
PIN33	IO35_L23P	M14
PIN34	IO35_L23N	M15
PIN35	IO35_L22P	L14
PIN36	IO35_L22N	L15
PIN37	GND	-
PIN38	GND	-
PIN39	+3.3V	-
PIN40	+3.3V	-

Part 7.4: Expansion Port J12

The expansion port J12 is a 40-pin 0.1 inch double-row connector, which expands more peripherals and interfaces for users. The default is not soldered, the user can solder to a double-row male connectors or female connectors as needed. The J12 interface can be directly connected to the module provided by ALINX. The expansion port J12, which expands more peripherals and interfaces for users. Currently, the J12 interface can be directly connected to the module provided by ALINX, include: ADDA module, LCD module, Gigabit Ethernet module, audio input/output module, matrix keyboard module, 500W binocular vision camera module, etc.

The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. 34 IO ports are connected to BANK34 and BANK35 of ZYNQ PL. The PCB design is differentially connected. The default level is 3.3V. The user can change the level of IO by replacing the power chip (SPX3819M5-3-3) of VCCIO34 and VCCIO35 on the core board.

Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.

The circuit of the expansion port (J12) is shown in Figure 7-7:

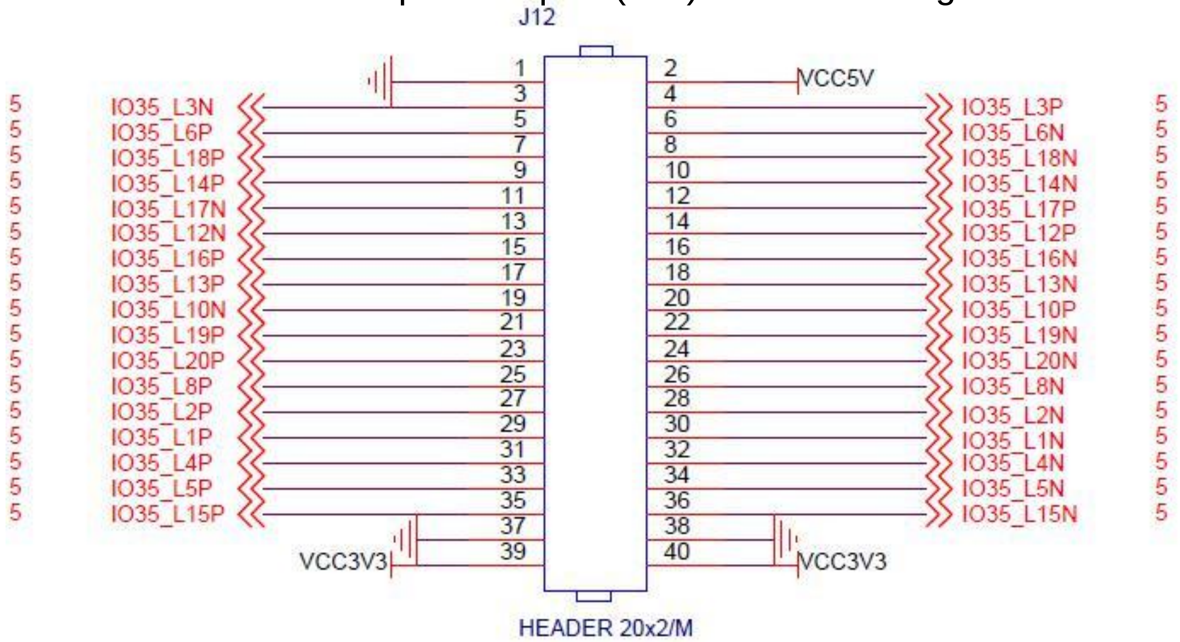


Figure 7-7: Expansion Port J12 schematic

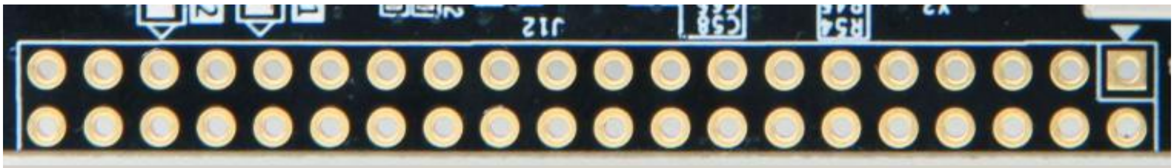


Figure 7-8: Expansion header J12 on the FPGA Board

J12 Expansion Header Pin Assignment

J11 Pin	Signal Name	ZYNQ Pin Number
PIN1	GND	-
PIN2	+5V	-
PIN3	IO35_L3N	D18
PIN4	IO35_L3P	E17
PIN5	IO35_L6P	F16
PIN6	IO35_L6N	F17
PIN7	IO35_L18P	G19
PIN8	IO35_L18N	G20
PIN9	IO35_L14P	J18
PIN10	IO35_L14N	H18
PIN11	IO35_L17N	H20
PIN12	IO35_L17P	J20
PIN13	IO35_L12N	K18
PIN14	IO35_L12P	K17
PIN15	IO35_L16P	G17
PIN16	IO35_L16N	G18
PIN17	IO35_L13P	H16
PIN18	IO35_L13N	H17
PIN19	IO35_L10N	J19
PIN20	IO35_L10P	K19
PIN21	IO35_L19P	H15
PIN22	IO35_L19N	G15
PIN23	IO35_L20P	K14
PIN24	IO35_L20N	J14
PIN25	IO35_L8P	M17
PIN26	IO35_L8N	M18
PIN27	IO35_L2P	B19
PIN28	IO35_L2N	A20
PIN29	IO35_L1P	C20
PIN30	IO35_L1N	B20
PIN31	IO35_L4P	D19
PIN32	IO35_L4N	D20
PIN33	IO35_L5P	E18
PIN34	IO35_L5N	E19

PIN35	IO35_L15P	F19
PIN36	IO35_L15N	F20
PIN37	GND	-
PIN38	GND	-
PIN39	+3.3V	-
PIN40	+3.3V	-